a second diffusion region, the second diffusion region couples the transistor to a bit line;

wherein the gate serves as a word line;

wherein the gate includes a buried portion and a non-buried portion, wherein the buried portion of the gate occupies the shallow transistor trench;

a gate dielectric having portions lining the shallow transistor trench; and

wherein one side of the gate dielectric is in contact with the buried portion of the gate and an opposite side of the gate dielectric is in contact with the first diffusion region.

## REMARKS

This is in response to the Office Action dated December 23, 2002.

The claims have been amended to point out that the gate includes a buried portion and a non-buried portion, wherein the buried portion of the gate occupies the shallow transistor trench; a gate dielectric having portions lining the shallow transistor trench; and wherein one side of the gate dielectric is in contact with the buried portion of the gate and an opposite side of the gate dielectric is in contact with the first diffusion region.

Such an arrangement is not described or suggested in Bronner et al.

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0845.

Respectfully submitted,

Date 2/25/03

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Attachment: Sheet showing changes made